AMENDMENTS TO THE CLAIMS

Claims 1-15 are pending in the present application. Claims 2 and 10 are canceled. Claims 1, 5, 6 and 9 are amended.

Claim Rejections under 35 U.S.C. §112

Claim 3 is amended as required by the Examiner to overcome the rejection under 35 U.S.C. §112.

Listing of Claims:

1. (Currently amended) A method to form a floating gate for a flash memory device, said method comprising:

forming a dielectric layer over a substrate;

removing a portion of said dielectric layer to define an area where said floating gate is to be formed;

forming a gate dielectric layer overlying ~~a substrate~~said dielectric layer and said area where said floating gate is to be formed, wherein the gate dielectric layer overlying said dielectric layer serve as a gate layer and said dielectric layer overlying said area where said floating gate is to be formed serves as a tunneling layer;

~~depositing~~forming a conductor layer overlying said gate dielectric layer;

~~depositing~~forming a masking layer overlying said ~~first~~ conductor layer;

forming conductive spacers on the sidewalls of said conductor layer and said masking layer wherein said spacers extend vertically above the top surface of said conductor layer; and

~~etching away~~removing said masking layer ~~to complete said floating gate~~.

2. (Canceled)

3. (Currently amended) The method according to Claim 1 wherein said ~~first~~ dielectric layer is formed by thermal oxidation of said substrate.

4. (Original) The method according to Claim 3 wherein said gate dielectric layer is formed by thermal oxidation of said substrate.

5. (Currently amended) The method according to Claim 1 wherein said ~~first and second~~ conductor layers and said conductive spacers comprise polysilicon.

6. (Currently amended) The method according to Claim 1 further comprising the steps of:

forming ~~a second~~another dielectric layer overlying said floating gate and said substrate;

forming ~~a third~~another conductor layer overlying said ~~second~~another dielectric layer; and

patterning said ~~third~~another conductor layer to form a control gate overlying said floating gate.

7. (Original) The method according to Claim 6 wherein part of said control gate overlies said substrate but not said floating gate.

8. (Original) The method according to Claim 7 further comprising implanting ions into said substrate to form doped regions adjacent to said control gate and to said floating gate.

9. (Currently amended) A method to form a flash memory device, said method comprising:

forming a first dielectric layer over a substrate;

removing a portion of said first dielectric layer to define an area where a floating gate is to be formed;

forming a gate dielectric layer overlying said fist dielectric layer and said area where said floating gate is to be formed, wherein the gate dielectric layer overlying said first dielectric layer serve as a gate layer, and said first dielectric layer overlying said area where said floating gate is to be formed serves as a tunneling layer~~a substrate~~;

~~depositing~~forming a first conductor layer overlying said gate dielectric layer;

~~depositing~~forming a masking layer overlying said first conductor layer;

~~etching through~~patterning said masking layer and said first conductor layer;

thereafter ~~depositing~~forming a second conductor layer overlying said masking layer, said first conductor layer, and said substrate;

~~etching down~~patterning said second conductor layer to form spacers on said sidewalls of said first conductor layer and said masking layer wherein said spacers extend vertically above the top surface of said first conductor layer;

~~etching away~~removing said masking layer ~~to complete said floating gate~~;

forming a second dielectric layer overlying said floating gate and said substrate;

forming a third conductor layer overlying said second dielectric layer; and

patterning said third conductor layer to form a control gate overlying said floating gate.

10. (Canceled)

11. (Original) The method according to Claim 9 wherein said first dielectric layer is formed by thermal oxidation of said substrate.

12. (Original) The method according to Claim 11 wherein said gate dielectric layer is formed by thermal oxidation of said substrate.

13. (Original) The method according to Claim 9 wherein said first and second conductor layers comprise polysilicon.

14. (Original) The method according to Claim 9 wherein part of said control gate overlies said substrate but not said floating gate.

15. (Original) The method according to Claim 14 further comprising implanting ions into said substrate to form doped regions adjacent to said control gate and to said floating gate.

16. (Withdrawn) A flash memory device comprising:

a substrate;

a floating gate overlying said substrate wherein said floating gate comprises:

a conductor layer overlying a dielectric layer; and

conductive spacers adjacent to and contacting said first conductor layer wherein said spacers extend vertically above said conductor layer; and

a control gate overlying said floating gate with a second dielectric therebetween.

17. (Withdrawn) The device according to Claim 16 wherein said gate dielectric layer underlying said floating gate comprises a first thickness underlying said first conductor layer and a second thickness underlying said spacers.

18. (Withdrawn) The device according to Claim 16 wherein said first and second conductor layers comprise polysilicon.

19. (Withdrawn) The device according to Claim 16 wherein part of said control gate overlies said substrate but not said floating gate.

20. (Withdrawn) The device according to Claim 19 further comprising doped regions adjacent to said control gate and to said floating gate.